

What is claimed is:

- 1 1. A frequency prescaler comprising:
2 a first sequential element having an input stage with at least one embedded
3 logic gate; and
4 a second sequential element having a clock input node coupled to an output
5 node of the first sequential element.
- 1 2. The frequency prescaler of claim 1 wherein the first sequential element is
2 coupled to perform a conditional divide-by-two operation.
- 1 3. The frequency prescaler of claim 1 further comprising a third sequential
2 element, and wherein the at least one logic gate is coupled to receive a signal from
3 the output node of the first sequential element and is coupled to receive a signal
4 from the third sequential element.
- 1 4. The frequency prescaler of claim 3 wherein the third sequential element is
2 coupled to decode a state of the first and second sequential elements.
- 1 5. The frequency prescaler of claim 4 wherein the third sequential element
2 includes at least one logic gate embedded within an input stage.
- 1 6. The frequency prescaler of claim 1 wherein the first sequential element
2 comprises a true single phase clock flip-flop.
- 1 7. The frequency prescaler of claim 1 wherein:
2 the first sequential element includes a clock input node configured to receive
3 a voltage controlled oscillator output signal; and
4 the first and second sequential elements are configured to form an
5 asynchronous counter.

1 8. The frequency prescaler of claim 7 further comprising a third sequential
2 element having an output node coupled to an input node of the at least one logic
3 gate of the first sequential element, and configured to decode a state of the
4 asynchronous counter.

1 9. The frequency prescaler of claim 8 wherein the third sequential element is
2 configured to be responsive to a control signal to conditionally lengthen a period of
3 the asynchronous counter by one cycle of the voltage controlled oscillator output
4 signal.

1 10. The frequency prescaler of claim 9 wherein the first sequential element
2 comprises a true single phase clock flip-flop.

1 11. The frequency prescaler of claim 9 wherein the third sequential element
2 comprises a true single phase clock flip-flop having an input stage with an
3 embedded logic gate.

1 12. An even/odd modulus prescaler comprising:
2 an asynchronous counter having a least significant stage clocked by an input
3 signal; and
4 a first true single phase clock flip-flop having an input stage with an
5 embedded logic gate to decode a state of the asynchronous counter, configured to
6 modify a modulus of the asynchronous counter between an even modulus and an
7 odd modulus.

1 13. The even/odd modulus prescaler of claim 12 wherein the least significant
2 stage of the asynchronous counter comprises a second true single phase clock flip-
3 flop having an input stage with an embedded logic gate.

1 14. The even/odd modulus prescaler of claim 13 wherein the embedded logic
2 gate of the least significant stage is coupled to receive signals from an output node
3 of the least significant stage and from the first true single phase clock flip-flop.

1 15. The even/odd modulus prescaler of claim 14 wherein the asynchronous
2 counter further comprises a more significant stage having a clock input node
3 coupled to the output node of the least significant stage.

1 16. The even/odd modulus prescaler of claim 12 wherein the asynchronous
2 counter comprises at least one additional more significant stage, wherein each of the
3 at least one additional more significant stage is configured to be clocked by a lesser
4 significant stage.

1 17. A frequency synthesizer comprising:
2 a comparison circuit to compare a reference signal and a frequency divided
3 signal;
4 a voltage controlled oscillator to synthesize an output signal in response to
5 the comparison circuit; and
6 a prescaler coupled to the voltage controlled oscillator to divide a frequency
7 of the output signal, wherein the prescaler includes an asynchronous divider with at
8 least one true single phase clock flip-flop having embedded logic in an input stage.

1 18. The frequency synthesizer of claim 17 wherein the at least one true single
2 phase clock flip-flop includes a least significant flip-flop coupled to be clocked by
3 the output signal, the least significant flip-flop including an input stage having an
4 embedded logic gate.

1 19. The frequency synthesizer of claim 18 wherein the at least one true single
2 phase clock flip-flop further includes a more significant flip-flop coupled to be
3 clocked by a signal produced by the least significant flip-flop.

1 20. The frequency synthesizer of claim 19 wherein the at least one true single
2 phase clock flip-flop further includes a decoder flip-flop to decode a state of the
3 least significant flip-flop and the more significant flip-flop.

1 21. The frequency synthesizer of claim 20 wherein the decoder flip-flop
2 comprises a true single phase clock flip-flop having an embedded logic gate to
3 decode the state.

1 22. The frequency synthesizer of claim 20 wherein the decoder flip-flop is
2 configured to be clocked by the output signal.

1 23. An electronic system that includes a direct conversion receiver with an
2 oscillator input port, a directional antenna coupled to the direct conversion receiver,
3 and a frequency synthesizer coupled to the oscillator input port, the frequency
4 synthesizer comprising:
5 a comparison circuit to compare a reference signal and a frequency divided
6 signal;
7 a voltage controlled oscillator to synthesize an output signal in response to
8 the comparison circuit; and
9 a prescaler coupled to the voltage controlled oscillator to divide a frequency
10 of the output signal, wherein the prescaler includes an asynchronous divider with at
11 least one true single phase clock flip-flop having embedded logic in an input stage.

1 24. The electronic system of claim 23 wherein the at least one true single phase
2 clock flip-flop includes a least significant flip-flop coupled to be clocked by the
3 output signal, the least significant flip-flop including an input stage having an
4 embedded logic gate.

1 25. The electronic system of claim 24 wherein the at least one true single phase
2 clock flip-flop further includes a more significant flip-flop coupled to be clocked by
3 a signal produced by the least significant flip-flop.

1 26. A method comprising:
2 clocking a first sequential element with an input signal, wherein the first
3 sequential element comprises a true single phase clock flip-flop;
4 clocking a second sequential element with an output signal from the first
5 sequential element;
6 decoding a state of the first and second sequential elements; and
7 conditionally gating an input signal to the first sequential element using a
8 logic gate embedded in an input stage of the true single phase clock flip-flop.

1 27. The method of claim 26 wherein decoding comprises receiving output
2 signals from the first and second sequential elements at a logic gate embedded in an
3 input stage of a third sequential element.

1 28. The method of claim 27 further comprising clocking the third sequential
2 element with the input signal.

1 29. The method of claim 26 wherein clocking a first sequential element with an
2 input signal comprises clocking the first sequential element with a voltage
3 controlled oscillator output signal.